Abstract of the Disclosure

In a multi-streaming processor having a memory cache, a system for fetching instructions from individual ones of multiple streams to an instruction pipeline is provided, comprising a fetch algorithm for selecting from which stream to fetch an instruction, and a hit/miss predictor for forecasting whether a load instruction will hit or miss the cache. The prediction by the hit-miss predictor is used by the fetch algorithm in determining from which stream to fetch. A hit prediction results in a next instruction being fetched from the same stream as the instruction tested by the hit/miss predictor, while a miss prediction results in the next instruction being fetched from a different stream, if any. The predictor is also used to determine which instructions to dispatch to functional units.